A Modified Apod Pulse Width Modulation Technique of Multilevel Cascaded Inverter Design

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Abstract – This paper proposes a Alternate Phase Opposition Disposition (APOD) strategy to achieve balanced line-to-line output voltages and to reduce the harmonic distortions by maximize the modulation index in the linear modulation range where the output voltage can be linearly adjusted in the multilevel cascaded inverter (MLCI) operating under unbalanced dc-link conditions. In these conditions, the linear modulation range is reduced, and a significant output voltage imbalance may occur as voltage references increase. Compared to the conventional multilevel inverter, the number of dc voltage sources, switches, installation area and converter cost is significantly reduced as the number of voltage steps increases. From this analysis, the theory behind the output voltage imbalance is explained, and the maximum linear modulation range considering an unbalanced dc-link condition is evaluated. After that, a Alternate Phase Opposition Disposition strategy is proposed to achieve output voltage balancing as well as to extend the linear modulation range up to the maximum reachable point in theory.Both the simulations and the experiments for a thirteen-level phase-shifted modulated MLCI for electric vehicle traction motor drive show that the proposed method is able to balance line-to-line output voltages as well as to maximize the linear modulation range under the unbalanced dc-link conditions.

Index Terms – Multilevel cascaded inverter (MLCI), pulse-width modulation (PWM), Alternate phase opposition disposition (APOD).

1. INTRODUCTION

Multilevel inverters enable the synthesis of a sinusoidal output voltage from several steps of voltages. For this reason, multilevel inverters have low dv/dt characteristics and generally have low harmonics in the output voltage and current. In addition, the switching of very high voltages can be achieved by stacking multilevel inverter modules. Due to these advantages, multilevel inverters have been applied in various application fields. Among various topologies for multilevel inverters, the multilevel cascaded inverter (MLCI) structure is one of the prominent topologies because of its simple structure for modularization and fault-tolerant capability. Therefore, MLCIs are used for many applications, such as dynamic voltage restorer, static synchronous compensator (STATCOM), high-voltage energy storage device, photovoltaic inverters, medium-voltage drives, electric vehicle (EV) traction drives, and so on In MLCI applications, a modulation strategy to generate gating signals is very crucial to achieve high-performance control.

Regarding this issue, many studies have been conducted, and they are roughly categorized into multilevel selective harmonic elimination pulse width modulation (SHEPWM), multilevel carrier-based PWM, and multilevel space vector (SVPWM) methods. Generally, a carrier-based PWM or SVPWM is preferred in applications such as motor drives, where dynamic properties are very important, whereas SHEPWM is preferred in some high-power static power conversion applications. To reduce the common-mode voltage, a multilevel SVPWM has been proposed. The series SVPWM method has been reported to easily implement SVPWM for the MLCI. SVPWM is proposed for hybrid inverters consisting of neutral point clamp and H-bridge inverters to improve output voltage quality and efficiency. As with two-level inverters, it is also possible to implement carrier-based SVPWMs which are equivalent to traditional SVPWMs by injecting a common offset voltage to the three-phase references.

Some methods to calculate the offset voltages to achieve the optimal space vector switching sequence are addressed. The performances of a carrier-based PWM and an SVPWM are compared, and a PWM scheme is proposed to obtain an optimal output voltage in the multilevel inverter. On the other hand, MLCIs require separated dc links. Therefore, if there is one or more faults present in the dc links in each phase, or if the voltage magnitudes of the dc links are unequal, the output voltage of the MLCI can be unbalanced without proper compensation. To resolve this issue, some studies have been conducted.

From the above equation it is shown that the available modulation index is reduced under faulty conditions on switch modules in multilevel inverters, and compensation algorithms

are proposed for alternate phase-disposition PWM and phase-shifted.

2. PROPOSED SYSTEM METHOD

A new hybrid topology is used for the multilevel inverter design. Hybrid topology is the combination of diode and the multilevel inverter. Alternate Phase opposition disposition (APOD) modulation- every carrier waveforms is in out of phase with its neighboring carrier by 180 degree. Harmonic distortions are reduced, when will increase the number of output levels and also reduce the switches.

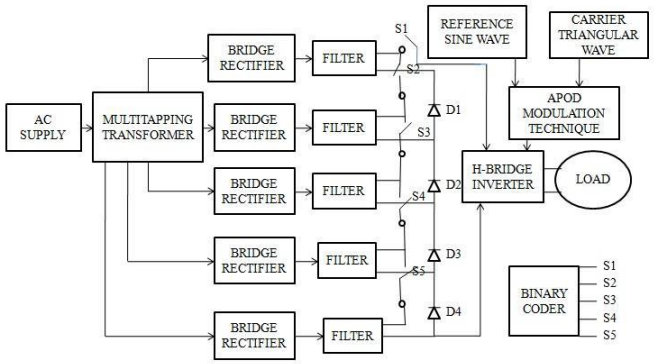

Fig.2.1 Block diagram of proposed method

Multi tapping transformer is used to divide the voltage level. Diode bridge rectifier is used to convert AC supply to DC supply and filter is used to removes the ripples.Binary coder gives the signal to switches, when the switches are connected to H bridge inverter.H bridge inverter is used to convert DC to AC and enables a voltage to across a load in either direction. Alternate Phase opposition disposition (APOD) modulation is used for voltage balancing.(every carrier waveforms is in out of phase with its neighboring carrier by 180). APOD produce the pulse signal to h bridge inverter.

3. ALTERNATE PHASE OPPOSITION DISPOSITION

In Alternate Phase Opposition Disposition Pulse Width Modulation (APOD), every carrier waveform is out phase with its neighboring carrier wave by 180 degree. All the carrier waveform have same frequency, same amplitude and but compare one carrier waveform to neighbor carrier waveform is phase shifted 180 degree. Odd carrier waveforms are in phase but compare to even carrier waveform are out of phase shift 180 degree in odd carrier waveform.

3.1. Alternate Phase Opposition Disposition Pulse Width Modulation

3.1.1 Sinusoidal Pulse Width Modulation

For Alternate phase opposition disposition (APOD) modulation , every carrier waveform is out phase with its neighboring carrier wave by 180 degree. The figure demonstrates the sine-triangle method for a five level inverter. Therein, the phase modulation signal is compared with four (N-1 in general) triangle waveforms.

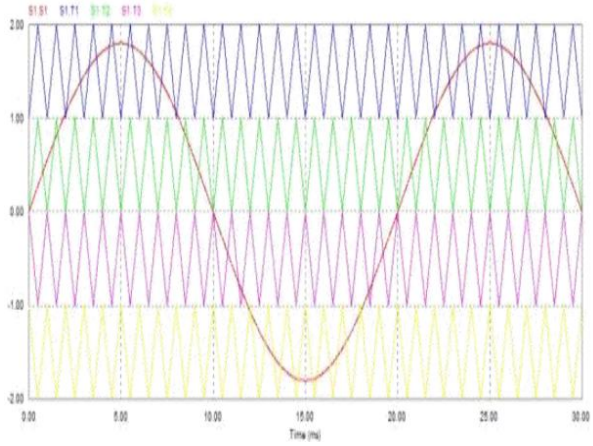

Fig 3.1 Waveform model for Alternate Phase opposition disposition sinusoidal pulse width modulation.

The rules for the alternate phase opposition disposition method, when the number of level N=5 are The N –1 = 4 carrier waveforms are arranged so that, every carrier waveform is out phase with its neighboring carrier wave by 180 degree.The converter is switches to +1 vdc when the reference is greater than all the carrier waveforms.The converter is switches to+2 vdc when the reference is less than the uppermost carrier waveform and greater than all other carriers.The converter is switches to ZERO when the reference is less than the two uppermost carrier waveform and greater than all other carriers.The converter is switches to -2 vdc when the reference is lesser than all the carrier waveforms.

In this technique, carrier waves with variable switching frequencies of 2KHz and 4KHz are compared with the reference wave of 50Hz as shown in Fig.

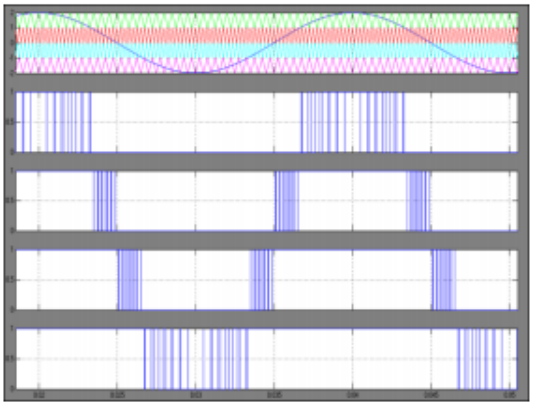

Fig 3.2 Waveform model for Alternate Phase opposition disposition sinusoidal pulse width modulation generation.

3.1.2. Sinusoidal with Zero Sequence Pulse Width Modulation

Fig. shows the sinusoidal pulse width modulation with zero sequence in which a triplen harmonic voltage is added to each of the reference waveforms.

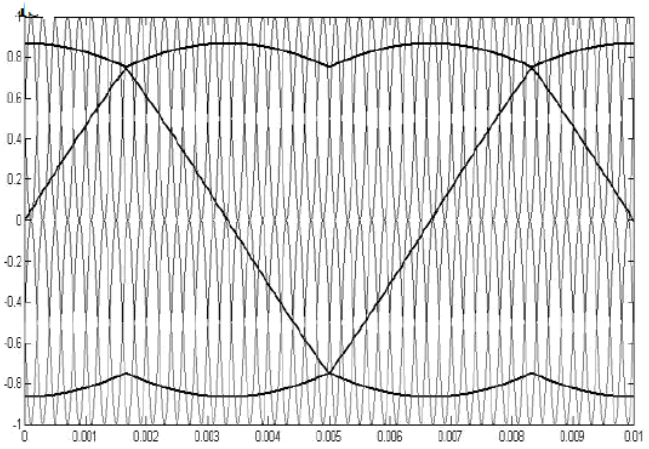

Fig 3.3 Waveform model for APOD sinusoidal with zero sequence pulse width modulation.

In this technique, carrier waves with variable switching frequencies of 2KHz and 4KHz are compared with the reference wave of 50Hz as shown in Fig.

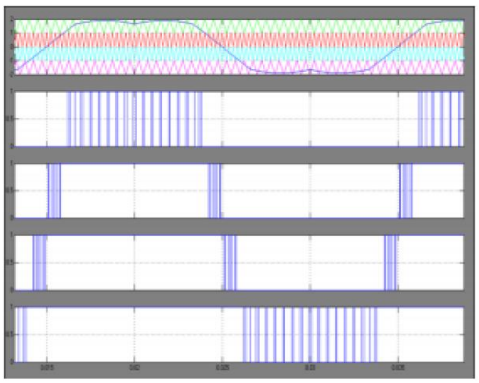

Fig 3.4 Alternate Phase opposition disposition sinusoidal with zero sequence pulse width modulation generation.

In this method all the carriers have the same frequency and the adjustable amplitude (different or unequal amplitudes).But every carrier waveform is out phase with its neighboring carrier wave by 180 degree Carrier and reference wave arrangements are as shown in Fig. 3.4

The converter is switched to +1 vdc when the sine wave is higher than all the carrier waveforms, the converter switches to +2 vdc when the sine wave is lower than the uppermost carrier waveform and greater than all other carrier, the converter is switched to zero when the sine wave is lesser than the two upper carrier waveform but greater than the lower carrier waveform, the converter switches to -1 vdc when the sine wave is higher than the lowermost carrier waveform and lesser than all other carriers and the converter is switched to -2 vdc when the sine wave is less than all the carrier waveforms.

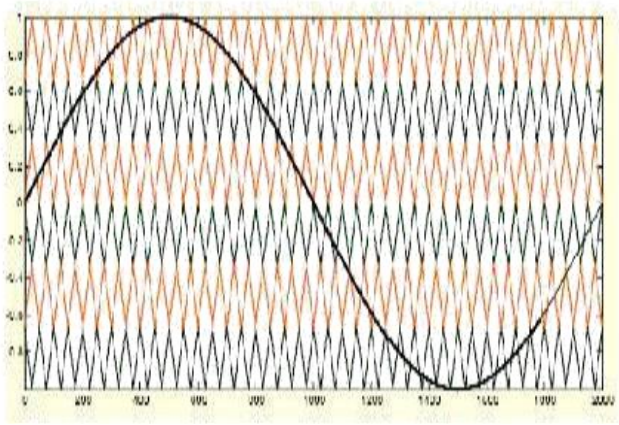

Fig 3.5 Carrier arrangement for APODPWM strategy

4. MULTILEVEL CASCADED INVERTER

4.1. Introduction

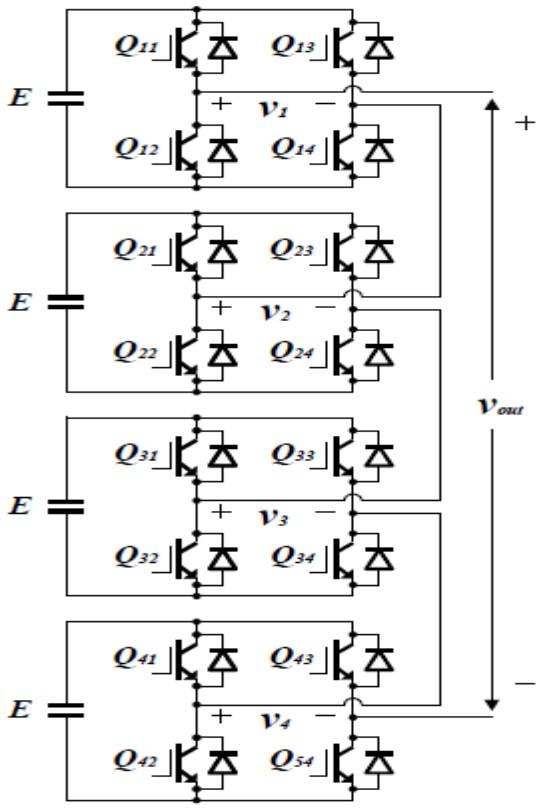

Fig 4.1 Circuit configuration of a conventional cascaded H-bridge multilevel inverter

The cascaded H-bridge multilevel inverter has been researched for high voltage applications since it has advantages in number of components, high reliability, and modularity. The main purpose of a multilevel inverter is the generation of a high voltage using lower voltage rating devices connected in series. Also it has the potential to get a high quality output voltage by producing multi output voltage levels. However, it increases the number of switching devices and other components, which results in an increase of complexity problems and system cost.

4.2. Operation and Properties

Many multilevel inverter configurations have been researched to get a sinusoidal-like output voltage wave with minimum circuit components. However, the configuration has brought a weakness in usage of high voltage applications due to its complexity in switch control and voltage stress (same as its input voltage source).

Fig shows a circuit configuration of a general cascaded H-bridge multilevel inverter. Each H-bridge module has an independent DC voltage source of *E*. Every output terminal of H-bridge cells is connected in series. So the output voltage can be obtained by Eq. (4.1). And the number of output voltage levels is obtained by Eq. (4.2).

$$V_{out} = \sum_{n=1}^{k} vn = V_1 + V_2 + V_3 + V_4. \quad (4.1)$$

$$N = 2k + 1 \quad (4.2)$$

where *k* is the number of H-bridge cells.

To reduce the number of switches, a multilevel inverter using a cascaded transformer has been introduced. A multilevel inverter employing a cascaded transformer. It has a single DC voltage source, two H-bridge cells, and two transformers. Since each secondary of the transformer is connected in series, the output voltage becomes the instantaneous sum of every secondary voltage of both transformers as given in Eq. (4.3). As well, the number of output voltage levels is determined by Eq. (4.4).

$$Vout = \sum_{n=0}^{k-1} 3n.Vn + 1 = V_1 + 3.V_2 \quad (4.3)$$

$$N = 3^k \quad (4.4)$$

where *k* is the number of transformers.

In Eq. (4.3), vn can be E, 0, or -E; therefore, vout can produce -4E, -3E, -2E, -E, 0, E, 2E, 3E, 4E by mixing of each secondary voltage of the transformers.

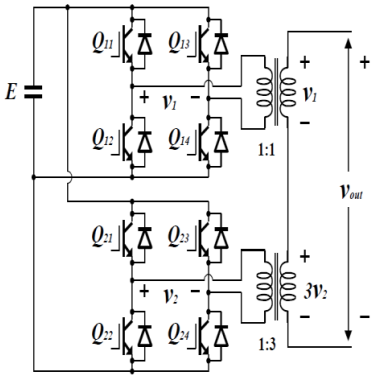

Fig 4.2 Circuit configuration of a multilevel inverter having a cascaded transformer

From above figure 4.2, we can find that this multilevel inverter saves 8 switches and 3 DC voltage sources compared with the prior approach given in Fig.4.1.It automatically achieves galvanic isolation between a source and loads by the cascaded transformer.

5. SIMULATION AND RESULTS

5.1. Simulation Circuit Diagram

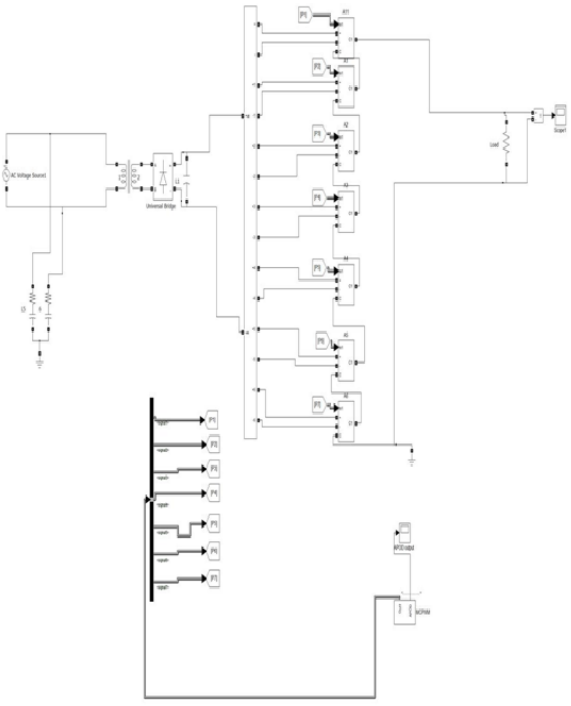

Fig 5.1 Simulation Circuit for Proposed System

Simulink, developed by Math Works, is a commercial tool for modeling, simulating and analyzing multi domain dynamic systems. Its primary interface is a graphical block diagramming

tool and a customizable set of block libraries. It offers tight integration with the rest of the MATLAB environment and can either drive MATLAB or be scripted from it. Simulink is widely used in control theory and digital signal processing for multi domain simulation and design.

A new hybrid topology is obtained at the simulation for the multi level inverter design in order to increase the reliability. Hybrid topology simulink diagram is designed as the combination of diode and the multi level inverter .Alternate Phase opposition disposition (APOD) modulation, every carrier waveforms is in out of phase with its neighboring carrier by 180 degree.

The number of output levels increased in the design so that the harmonic distortions are reduced and also reduce the switches. Multi tapping transformer is designed to divide the voltage level. Diode bridge rectifier is connected to AC supply in order to convert AC supply to DC supply and filter model is used to removes the ripples.Binary coder gives the signal to switches, when the switches are connected to H bridge inverter. The H bridge inverter model is used to convert DC to AC and enables a voltage to across a load in either direction. Alternate Phase opposition disposition (APOD) modulation is used for voltage balancing.(every carrier waveforms is in out of phase with its neighboring carrier by 180). APOD produces the pulse signal to H bridge inverter design.

5.2. Subsystem

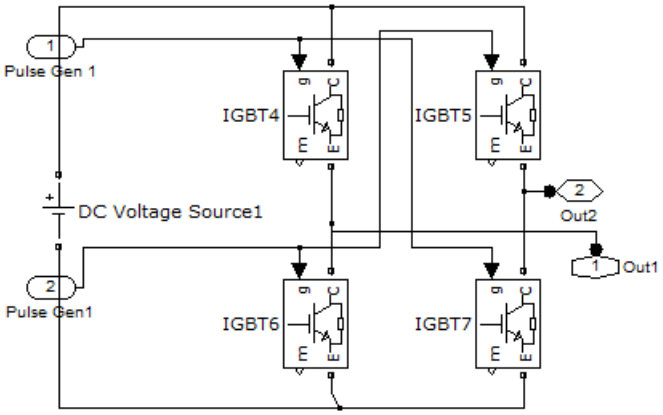

Fig 5.2 Subsystem of inverter

5.3. Specifications

Peak amplitude – 240 V

Frequency - 50 HZ

Carrier wave frequency - 250 HZ

Reference wave frequency – 50 HZ

%THD OF PWM	12%
%THD OF NVM	7.8%
%THD OF APOD	4.13%

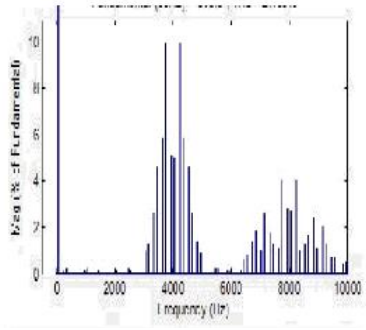

Fig 5.3 %THD of APOD pwm technique.

6. RESULTS

The various level of input wave diagrams from the Simulation results are described below.

6.1. Pulse output from APOD

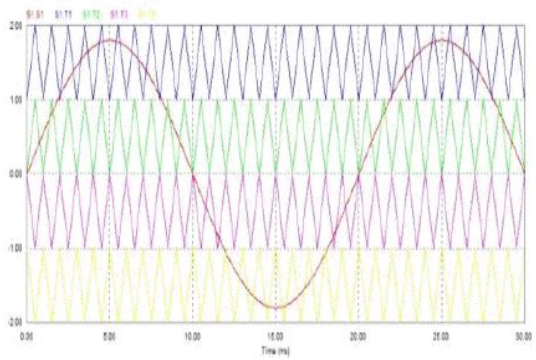

Fig 6.1 Pulse output

6.2. Multilevel Inverter output voltage

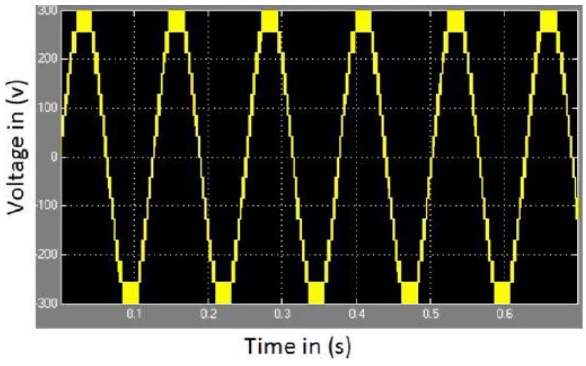

Fig 6.2 Multilevel Inverter output Voltage

7. CONCLUSION

The APOD technique for MLCIs under unbalanced dc-link conditions has been proposed in this paper. In order to analyze the maximum synthesizable voltage of MLCIs, the voltage vector space has been analyzed using the switching function. From the analysis, the maximum linear modulation range was derived. The proposed APOD technique is applied to achieve the maximum modulation index in the linear modulation range under an unbalanced dc-link condition as well as to balance the output phase voltages. Compared to the previous methods, the proposed technique is easily implemented and improves the output voltage quality under unbalanced dc-link conditions. The number of output levels increased in the design so that the harmonic distortions are reduced and also reduce the switches. Both simulation and experimental results based on the universal motor drive application verify the effectiveness of the proposed method.

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